Amendments to the Claims:

This listing of claims replaces all prior versions, and all prior listings, of claims in the application.

Listing of Claims:

1. (currently amended) A fabrication method of a semiconductor integrated circuit device, comprising the steps of:

(a) depositing a silicon nitride insulating film over a semiconductor substrate;

(b) depositing a silicon oxide insulating film over said silicon nitride insulating film; and

(c) subjecting said semiconductor substrate to a plasma etching treatment using an etching gas containing a fluorocarbon gas, oxygen and a dilution gas to process said silicon oxide insulating film,

wherein a residence time of the etching gas within an etching chamber is set at 50 to 700 ms, and

wherein a temperature of said semiconductor substrate ~~being~~ during the plasma ~~etched~~ etching treatment ranges from ~~60~~ 100° to ~~140°C~~130°C.

2. (currently amended) A method according to Claim 1, wherein a pressure within the etching chamber during ~~the course of~~ the plasma etching treatment ranges from 0.7 to 7 Pa.

3. (original) A method according to Claim 1, wherein a total flow rate of the etching gas passed into the etching chamber ranges from 200 to 1000 cm^3/minute.

4. (original) A method according to Claim 1, wherein a total flow rate of the etching gas passed into the etching chamber is at 700 cm^3/minute or over.

5. (original) A method according to Claim 1, wherein a pressure within the etching chamber during the plasma etching ranges from 1.3 to 4 Pa, and the total flow rate of the etching gas passing into the etching chamber is at 700 cm^3/minute or over.

6. (original) A method according to Claim 1, wherein a flow rate of said dilution gas is larger than the flow rates of said fluorocarbon gas and oxygen.

Claims 7 and 8 (canceled)

9. (original) A method according to Claim 1, wherein a plasma density during the plasma etching ranges from 1×10^{10} to $1 \times 10^{13}/cm^3$.

10. (original) A method according to Claim 1, wherein a plasma density during the plasma etching ranges from 1×10^{10} to $1 \times 10^{12}/cm^3$.

11. (original) A method according to Claim 1, wherein said fluorocarbon gas is made of C_5F_8, and said dilution gas is made of argon.

12. (original) A method according to Claim 11, wherein a flow rate of said argon gas ranges from 200 to 1000 cm^3/minute.

13. (previously presented) A method according to Claim 11, wherein a flow rate of said argon gas ranges from 400 to 800 cm^3/minute.

14. (original) A method according to Claim 11, wherein a ratio in flow rate between the oxygen and C_5F_8 (oxygen/C_5F_8) ranges from 0.8 to 1.5.

15. (original) A method according to Claim 11, wherein a ratio in flow rate between the oxygen and C_5F_8 (oxygen/C_5F_8) ranges from 1 to 1.2.

16. (original) A method according to Claim 11, wherein a partial pressure of C_5F_8 ranges from 0.02 to 0.2 Pa.

17. (original) A method according to Claim 11, wherein a partial pressure of C_5F_8 ranges from 0.04 to 0.1 Pa.

18. (currently amended) A fabrication method of a semiconductor integrated circuit device, comprising the steps of:

(a) depositing a silicon nitride insulating film over a semiconductor substrate;

(b) depositing a silicon oxide insulating film over said silicon nitride insulating film; and

(c) subjecting said semiconductor substrate to a plasma etching treatment using an etching gas containing a fluorocarbon gas, oxygen and a dilution gas to process said silicon oxide insulating film,

wherein a residence time of the etching gas within an etching chamber is set at 50 to 350 ms, and

wherein a temperature of said semiconductor substrate ~~being~~ during the plasma ~~etched~~ etching treatment ranges from ~~60~~ 100° to ~~140°C~~130°C.

19. (currently amended) A fabrication method of a semiconductor integrated circuit device, comprising the steps of:

(a) depositing a silicon nitride insulating film over a semiconductor substrate;

(b) depositing a silicon oxide insulating film over said silicon nitride insulating film; and

(c) subjecting said semiconductor substrate to a plasma etching treatment using an etching gas containing a fluorocarbon gas, oxygen and a dilution gas to process said silicon oxide insulating film,

wherein a residence time of said etching gas within an etching chamber is set at 100 to 200 ms, and

wherein a temperature of said semiconductor substrate ~~being~~ during the plasma ~~etched~~ etching treatment ranges from ~~60~~ 100° to ~~140°C~~130°C.

20. (currently amended) A fabrication method of a semiconductor integrated circuit device, comprising the steps of:

(a) depositing a silicon nitride insulating film over a semiconductor substrate;

(b) depositing a silicon oxide insulating film over said silicon nitride insulating film; and

(c) subjecting said silicon oxide insulating film to a plasma etching treatment using an etching gas containing a fluorocarbon gas, oxygen and a dilution gas to process said silicon oxide insulating film,

wherein a pressure within an etching chamber during the plasma etching treatment ranges from 0.7 to 7 Pa, and a total flow rate of the etching gas passed into said etching chamber is 700 cm^3/minute or over, and

wherein a temperature of said semiconductor substrate ~~being~~ during the plasma ~~etched~~ etching treatment ranges from ~~60~~ 100° to ~~140°C~~130°C.

21. (currently amended) A fabrication method of a semiconductor integrated circuit device, comprising the steps of:

(a) depositing a silicon nitride insulating film over a semiconductor substrate;

(b) depositing a silicon oxide insulating film over said silicon nitride insulating film; and

(c) subjecting said silicon oxide insulating film to a plasma etching treatment using an etching gas containing a fluorocarbon gas, oxygen and a dilution gas to process said silicon oxide insulating film,

wherein a pressure within said etching chamber during the plasma etching ranges from 1.3 to 4 Pa, and a total flow rate of said etching gas passed into the etching chamber is at 700 cm^3/minute or over, and

wherein a temperature of said semiconductor substrate ~~being~~ during the plasma ~~etched~~ etching treatment ranges from ~~60~~ 100° to ~~140°C~~130°C.

22. (currently amended) A fabrication method of a semiconductor integrated circuit device, comprising the steps of:

(a) depositing a silicon oxide insulating film over a patterned silicon nitride film with a doped polycrystalline silicon plug over a semiconductor substrate;

(b) forming a hard mask over said silicon oxide insulating film; and

(c) subjecting said semiconductor substrate to a plasma etching treatment through the hard mask as an etching mask using an etching gas containing a fluorocarbon gas, oxygen and a dilution gas to process said silicon oxide insulating film, so as to form a hole in said silicon oxide insulating film down to the patterned silicon nitride film in such a manner that an upper surface of the doped polycrystalline silicon plug is exposed,

wherein a residence time of the etching gas within an etching chamber is set at 50 to 700 ms.

23. (original) A method according to Claim 22, wherein a pressure within the chamber during the plasma etching ranges from 0.7 to 7 Pa.

24. (original) A method according to Claim 22, wherein a total flow rate of the etching gas passed into the etching chamber ranges from 200 to 1000 cm^3/minute.

25. (original) A method according to Claim 22, wherein a total flow rate of the etching gas passed into the etching chamber is at 700 cm^3/minute or over.

26. (original) A method according to Claim 22, wherein a pressure within the etching chamber during the plasma etching ranges from 1.3 to 4 Pa, and the total flow rate of the etching gas passing into the etching chamber is at 700 cm^3/minute or over.

27. (original) A method according to Claim 22, wherein a flow rate of said dilution gas is larger than the flow rates of said fluorocarbon gas and oxygen.

28. (original) A method according to Claim 22, wherein a plasma density during the plasma etching ranges from 1×10^{10} to $1 \times 10^{13}/cm^3$.

29. (original) A method according to Claim 22, wherein a plasma density during the plasma etching ranges from 1×10^{10} to $1 \times 10^{12}/cm^3$.

30. (original) A method according to Claim 22, wherein said fluorocarbon gas is made of C_5F_8, and said dilution gas is made of argon.

31. (original) A method according to Claim 30, wherein a flow rate of said argon gas ranges from 200 to 1000 cm^3/minute.

32. (original) A method according to Claim 30, wherein a flow rate of said argon gas ranges from 400 to 800 cm^3/minute.

33. (original) A method according to Claim 30, wherein a ratio in flow rate between the oxygen and C_5F_8 (oxygen/C_5F_8) ranges from 0.8 to 1.5.

34. (original) A method according to Claim 30, wherein a ratio in flow rate between the oxygen and C_5F_8 (oxygen/C_5F_8) ranges from 1 to 1.2.

35. (original) A method according to Claim 30, wherein a partial pressure of C_5F_8 ranges from 0.02 to 0.2 Pa.

36. (original) A method according to Claim 30, wherein a partial pressure of C_5F_8 ranges from 0.04 to 0.1 Pa.

37. (currently amended) A fabrication method of a semiconductor integrated circuit device, comprising the steps of:

(a) depositing a silicon oxide insulating film over a patterned silicon nitride film with a doped polycrystalline silicon plug over a semiconductor substrate;

(b) forming a hard mask over said silicon oxide film; and

(c) subjecting the semiconductor substrate to a plasma etching treatment through the hard mask as an etching mask using an etching gas containing a fluorocarbon gas, oxygen and a dilution gas to process said silicon oxide insulating film, so as to form a hole in said silicon oxide insulating film down to the patterned silicon nitride film in such a manner that an upper surface of the doped polycrystalline silicon plug is exposed,

wherein a residence time of the etching gas within an etching chamber is set at 50 to 350 ms.

38. (currently amended) A fabrication method of a semiconductor integrated circuit device, comprising the steps of:

(a) depositing a silicon oxide insulating film over a patterned silicon nitride film with a doped polycrystalline silicon plug over a semiconductor substrate;

(b) forming a hard mask over said silicon oxide film; and

(c) subjecting the semiconductor substrate to a plasma etching treatment through the hard mask as an etching mask using an etching gas containing a fluorocarbon gas, oxygen and a dilution gas to process said silicon oxide insulating film, so as to form a hole in said silicon oxide insulating film down to the patterned silicon nitride film in such a manner that an upper surface of the doped polycrystalline silicon plug is exposed,

wherein a residence time of the etching gas within an etching chamber is set at 100 to 200 ms.

39. (currently amended) A fabrication method of a semiconductor integrated circuit device, comprising the steps of:

(a) depositing a silicon oxide insulating film over a patterned silicon nitride film with a doped polycrystalline silicon plug over a semiconductor substrate;

(b) forming a hard mask over said silicon oxide film; and

(c) subjecting the semiconductor substrate to a plasma etching treatment through the hard mask as an etching mask using an etching gas containing a fluorocarbon gas, oxygen and a dilution gas to process said silicon oxide insulating film, so as to form a hole in said silicon oxide insulating film down to the patterned silicon nitride film in such a manner that an upper surface of the doped polycrystalline silicon plug is exposed,

wherein a pressure within the etching chamber during the plasma etching ranges from 0.7 to 7 Pa and a total flow rate of the etching gas passed into the etching chamber is 700 cm^3/minute or over.

40. (currently amended) A fabrication method of a semiconductor integrated circuit device, comprising the steps of:

(a) depositing a silicon oxide insulating film over a patterned silicon nitride film with a doped polycrystalline silicon plug over a semiconductor substrate;

(b) forming a hard mask over said silicon oxide film; and

(c) subjecting the semiconductor substrate to a plasma etching treatment through the hard mask as an etching mask using an etching gas containing a fluorocarbon gas, oxygen and a dilution gas to process said

silicon oxide insulating film, so as to form a hole in said silicon oxide insulating film down to the patterned silicon nitride film in such a manner that an upper surface of the doped polycrystalline silicon plug is exposed,

wherein a pressure within the etching chamber during the plasma etching ranges from 1.3 to 4 Pa and a total flow rate of the etching gas passed into the etching chamber is 700 cm^3/minute or over.